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(54) SEMICONDUCTOR DEVICE

(57) Abstract

PURPOSE: To prevent latch-up without increasing the chip size by arranging a first diffusion region, a first well region and a second diffusion region in parallel while spaced apart from each other between the inner logic circuit and the peripheral circuit region such that the inner circuit region is surrounded.

CONSTITUTION: Fluctuation of potential is suppressed on an N type semiconductor substrate 100 and in a P type second well region in order to reduce the voltage appearing across a parasitic resistance, corresponding to resistances r1 and r2, existing between the N type semiconductor substrate 100 and the P type second well region. A P type second diffusion region 2 is thereby provided in an N type first diffusion region and a P type first well region 22 provided between an inner logic circuit region 5 and a peripheral circuit region 6. This structure eliminates the latch-up between the inner logic circuit region 5 and the peripheral circuit region 6 and exhibits the function sufficiently without increasing the chip size.